Integrated Synthesizer and VCO

ADF4360-7

FEATURES

Output frequency range: 350 MHz to 1800 MHz
Divide-by-2 output
3.0 V to 3.6 V power supply
1.8 V logic compatibility
Integer-N synthesizer
Programmable dual-modulus prescaler 8/9, 16/17
Programmable output power level
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode

APPLICATIONS

Wireless handsets (DECT, GSM, PCS, DCS, WCDMA)
Test equipment
Wireless LANs
CATV equipment

GENERAL DESCRIPTION

The ADF4360-7 is an integrated integer-N synthesizer and voltage controlled oscillator (VCO). The ADF4360-7 center frequency is set by external inductors. This allows a frequency range of between 350 MHz to 1800 MHz. In addition, a divide-by-2 option is available, whereby the user receives an RF output of between 175 MHz and 900 MHz.

Control of all the on-chip registers is through a simple 3-wire interface. The device operates with a power supply ranging from 3.0 V to 3.6 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

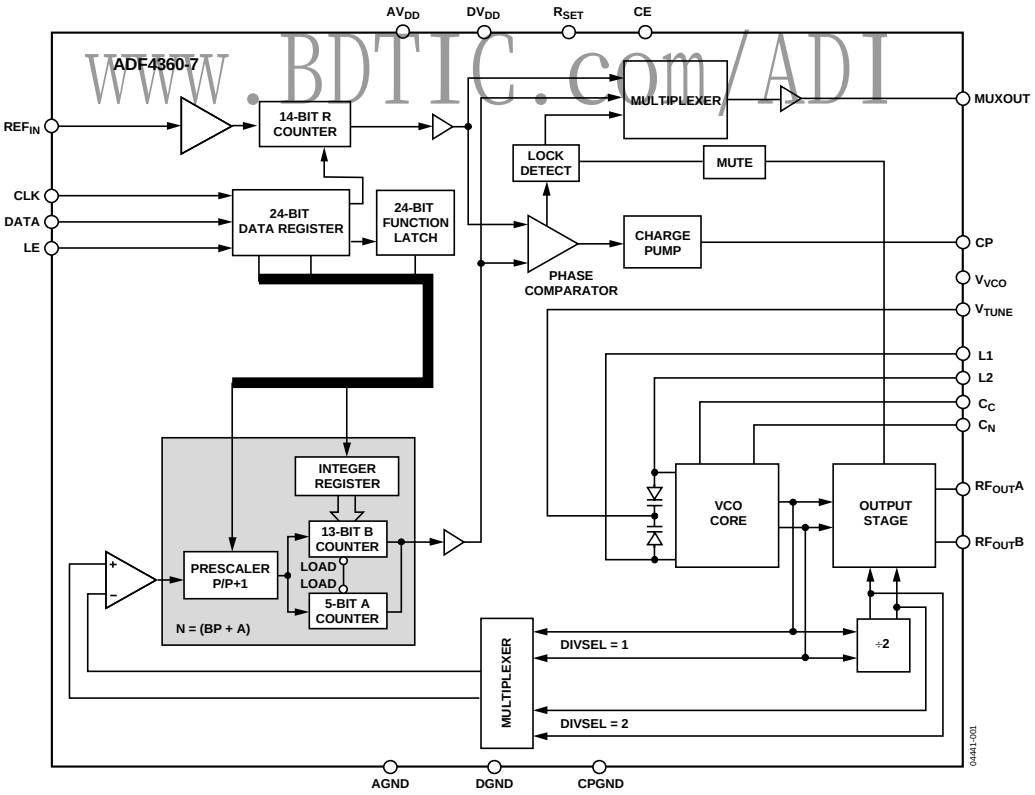

Figure 1.

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Rev. A

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REVISION HISTORY

11/04—Rev. 0 to Rev. A.

Updated Format ... Universal
Changes to General Description ... 1
Changes to Specifications ... 3
Changes to the Reference Input Section ... 10
Changes to Power-Up Section ... 17
Added Table 10 ... 17
Added Figure 22 ... 17
Updated Outline Dimensions ... 25

2/04—Revision 0: Initial Version.

SPECIFICATIONS[1]

AV_{DD} = DV_{DD} = V_{VCO} = 3.3 V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version	Unit	Conditions/Comments
REF_{IN} CHARACTERISTICS			
REF_{IN} Input Frequency	10/250	MHz min/max	For f < 10 MHz, use a dc-coupled CMOS-compatible square wave, slew rate > 21 V/µs.
REF_{IN} Input Sensitivity	0.7/AV_{DD}	V p-p min/max	AC-coupled.
	0 to AV_{DD}	V max	CMOS compatible.
REF_{IN} Input Capacitance	5.0	pF max	
REF_{IN} Input Current	±60	µA max	
PHASE DETECTOR			
Phase Detector Frequency[2]	8	MHz max	
CHARGE PUMP			
I_{CP} Sink/Source[3]			With R_{SET} = 4.7 kΩ.
High Value	2.5	mA typ	
Low Value	0.312	mA typ	
R_{SET} Range	2.7/10	kΩ	
I_{CP} Three-State Leakage Current	0.2	nA typ	
Sink and Source Current Matching	2	% typ	1.25 V ≤ V_{CP} ≤ 2.5 V.
I_{CP} vs. V_{CP}	1.5	% typ	1.25 V ≤ V_{CP} ≤ 2.5 V.
I_{CP} vs. Temperature	2	% typ	V_{CP} = 2.0 V.
LOGIC INPUTS			
V_{INH}, Input High Voltage	1.5	V min	
V_{INL}, Input Low Voltage	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	3.0	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	DV_{DD} – 0.4	V min	CMOS output chosen.
I_{OH}, Output High Current	500	µA max	
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = 500 µA.
POWER SUPPLIES			
AV_{DD}	3.0/3.6	V min/V max	
DV_{DD}	AV_{DD}		
V_{VCO}	AV_{DD}		
AI_{DD}[4]	10	mA typ	
DI_{DD}[4]	2.5	mA typ	
I_{VCO}[4, 5]	14.0	mA typ	I_{CORE} = 5 mA.
I_{RFOUT}[4]	3.5 to 11.0	mA typ	RF output stage is programmable.
Low Power Sleep Mode	7	µA typ	

Specifications continued on next page.

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Parameter	B Version	Unit	Conditions/Comments
RF OUTPUT CHARACTERISTICS[5]			
Maximum VCO Output Frequency	1800	MHz	I_{CORE} = 5 mA. Depending on L. See the Choosing the Correct Inductance Value section.
Minimum VCO Output Frequency	350	MHz	
VCO Output Frequency	490/585	MHz min/max	L1, L2 = 13 nH. See the Choosing the Correct Inductance Value section for other frequency values.
VCO Frequency Range	1.2	Ratio	F_{MAX}/F_{MIN}
VCO Sensitivity	12	MHz/V typ	L1, L2 = 13 nH. See the Choosing the Correct Inductance Value section for other sensitivity values.
Lock Time[6]	400	µs typ	To within 10 Hz of final frequency.
Frequency Pushing (Open Loop)	6	MHz/V typ	
Frequency Pulling (Open Loop)	15	kHz typ	Into 2.00 VSWR load.
Harmonic Content (Second)	−19	dBc typ	
Harmonic Content (Third)	−9	dBc typ	
Output Power[5, 7]	−14/−5	dBm typ	Programmable in 3 dB steps. See Table 7.
Output Power Variation	±3	dB typ	For tuned loads, see Output Matching section.
VCO Tuning Range	1.25/2.5	V min/max	
NOISE CHARACTERISTIC[5]			
VCO Phase-Noise Performance[8]	−116	dBc/Hz typ	@ 100 kHz offset from carrier.
	−138	dBc/Hz typ	@ 1 MHz offset from carrier.
	−144	dBc/Hz typ	@ 3 MHz offset from carrier.
	−148	dBc/Hz typ	@ 10 MHz offset from carrier.
Synthesizer Phase-Noise Floor[9]	−172	dBc/Hz typ	@ 25 kHz PFD frequency.
	−163	dBc/Hz typ	@ 200 kHz PFD frequency.
	−147	dBc/Hz typ	@ 8 MHz PFD frequency.
In-Band Phase Noise[10, 11]	−92	dBc/Hz typ	@ 1 kHz offset from carrier.
RMS Integrated Phase Error[12]	0.3	Degrees typ	100 Hz to 100 kHz.
Spurious Signals due to PFD Frequency[11, 13]	−70	dBc typ	
Level of Unlocked Signal with MTLD Enabled	−44	dBm typ	

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[1] Operating temperature range is −40°C to +85°C.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] I_{CP} is internally modified to maintain constant loop gain over the frequency range.
[4] T_A = 25°C; AV_{DD} = DV_{DD} = V_{VCO} = 3.3 V; P = 32.
[5] Unless otherwise stated, these characteristics are guaranteed for VCO core power = 5 mA. L1, L2 = 13 nH, 470 Ω resistors to GND in parallel with L1, L2.
[6] Jumping from 490 MHz to 585 MHz. PFD frequency = 200 kHz; loop bandwidth = 10 kHz.
[7] Using 50 Ω resistors to V_{VCO}, into a 50 Ω load. For tuned loads, see the Output Matching section.
[8] The noise of the VCO is measured in open-loop conditions.
[9] The synthesizer phase-noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value).
[10] The phase noise is measured with the EVAL-ADF4360-xEB1 Evaluation Board and the HP 8562E Spectrum Analyzer. The Spectrum Analyzer provides the REF_{IN} for the synthesizer; offset frequency = 1 kHz.
[11] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; N = 2500; loop B/W = 10 kHz.
[12] f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; N = 500; loop B/W = 25 kHz.
[13] The spurious signals are measured with the EVAL-ADF4360-xEB1 Evaluation Board and the HP 8562E Spectrum Analyzer. The Spectrum Analyzer provides the REF_{IN} for the synthesizer; f_{REFOUT} = 10 MHz @ 0 dBm.

TIMING CHARACTERISTICS[1]

AV_{DD} = DV_{DD} = V_{VCO} = 3.3 V ± 10%; AGND = DGND = 0 V; 1.8 V and 3 V logic levels used; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE Setup Time
t_2	10	ns min	DATA to CLOCK Setup Time
t_3	10	ns min	DATA to CLOCK Hold Time
t_4	25	ns min	CLOCK High Duration
t_5	25	ns min	CLOCK Low Duration
t_6	10	ns min	CLOCK to LE Setup Time
t_7	20	ns min	LE Pulse Width

[1] Refer to the Power-Up section for the recommended power-up procedure for this device.

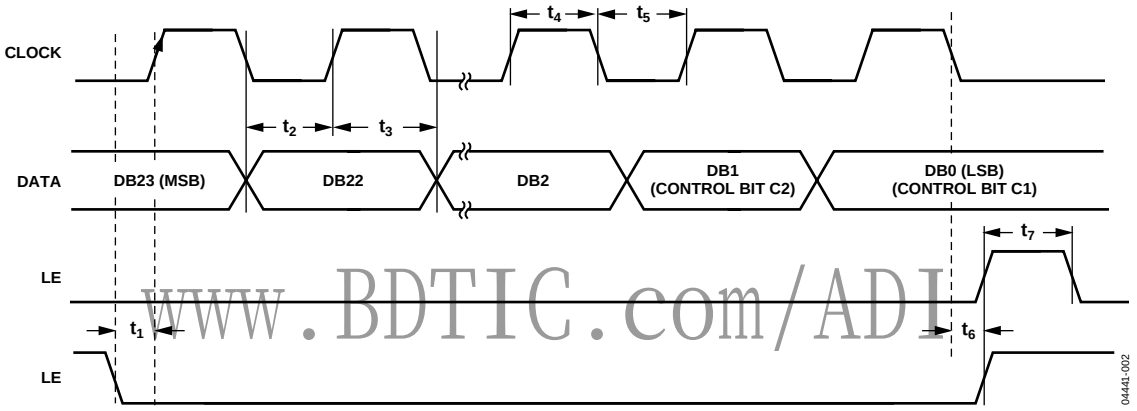

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Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.9 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_{VCO} to GND	−0.3 V to +3.9 V
V_{VCO} to AV_{DD}	−0.3 V to +0.3 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Maximum Junction Temperature	150°C
CSP θ_{JA} Thermal Impedance	
Paddle Soldered	50°C/W
Paddle Not Soldered	88°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <1 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

TRANSISTOR COUNT

12543 (CMOS) and 700 (Bipolar)

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ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

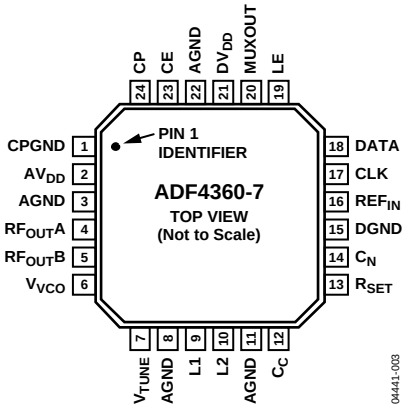

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
2	AV_{DD}	Analog Power Supply. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must have the same value as DV_{DD}.
3, 8, 11, 22	AGND	Analog Ground. This is the ground return path of the prescaler and VCO.
4	$RF_{OUT}A$	VCO Output. The output level is programmable from −5 dBm to −14 dBm. See the Output Matching section for a description of the various output stages.
5	$RF_{OUT}B$	VCO Complementary Output. The output level is programmable from −5 dBm to −14 dBm. See the Output Matching section for a description of the various output stages.
6	V_{VCO}	Power Supply for the VCO. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. V_{VCO} must have the same value as AV_{DD}.
7	V_{TUNE}	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP output voltage.
9	L1	An external inductor to AGND should be connected to this pin to set the ADF4360-7 output frequency. L1 and L2 need to be the same value. For inductances greater than 3.3 nH, a 470 Ω resistor should be added in parallel to AGND.
10	L2	An external inductor to AGND should be connected to this pin to set the ADF4360-7 output frequency. L1 and L2 need to be the same value. For inductances greater than 3.3 nH, a 470 Ω resistor should be added in parallel to AGND.
12	C_C	Internal Compensation Node. This pin must be decoupled to ground with a 10 nF capacitor.
13	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current for the synthesizer. The nominal voltage potential at the R_{SET} pin is 0.6 V. The relationship between I_{CP} and R_{SET} is $$I_{CPmax} = \frac{11.75}{R_{SET}}$$ where R_{SET} = 4.7 kΩ, and I_{CPmax} = 2.5 mA.
14	C_N	Internal Compensation Node. This pin must be decoupled to V_{VCO} with a 10 µF capacitor.
15	DGND	Digital Ground.
16	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ (see Figure 16). This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
17	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
18	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
19	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, and the relevant latch is selected using the control bits.
20	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
21	DV_{DD}	Digital Power Supply. This ranges from 3.0 V to 3.6 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must have the same value as AV_{DD}.
23	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. Taking the pin high powers up the device depending on the status of the power-down bits.
24	CP	Charge Pump Output. When enabled, this provides ± I_{CP} to the external loop filter, which in turn drives the internal VCO.

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TYPICAL PERFORMANCE CHARACTERISTICS

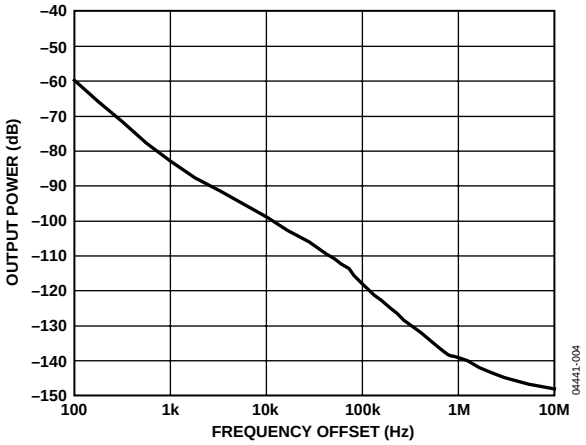

Figure 4. Open-Loop VCO Phase Noise, L1, L2 = 13 nH

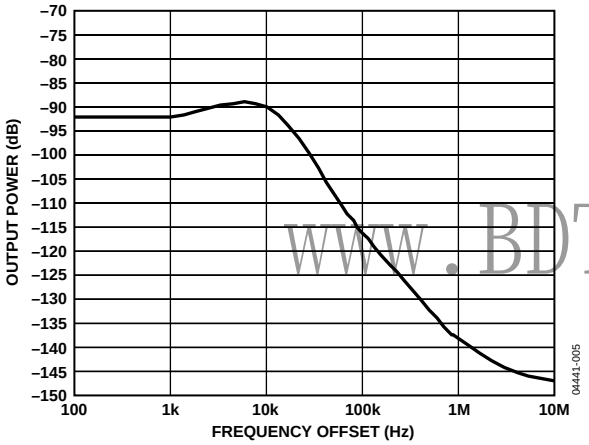

Figure 5. VCO Phase Noise, 500 MHz, 200 kHz PFD, 10 kHz Loop Bandwidth

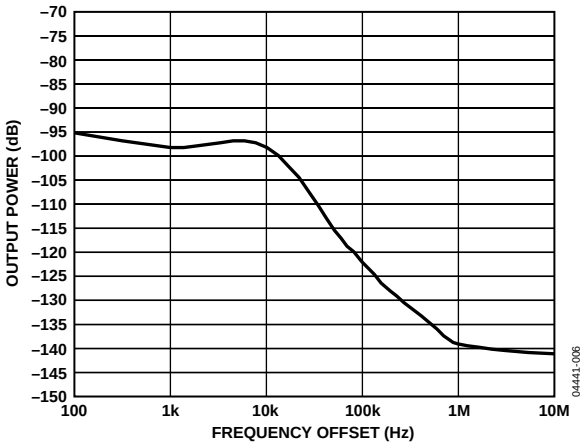

Figure 6. VCO Phase Noise, 250 MHz, Divide-by-2 Enabled 200 kHz PFD, 10 kHz Loop Bandwidth

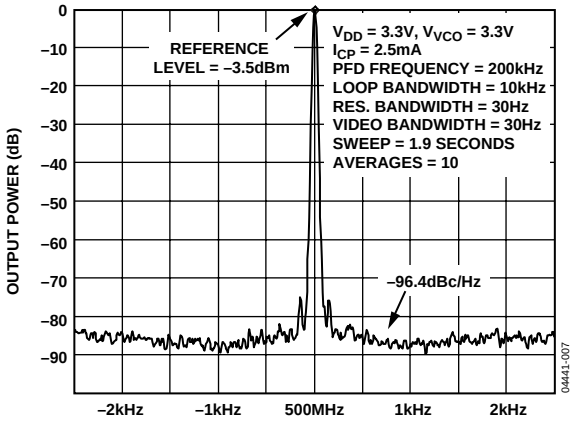

Figure 7. Close-In Phase Noise at 500 MHz (200 kHz Channel Spacing)

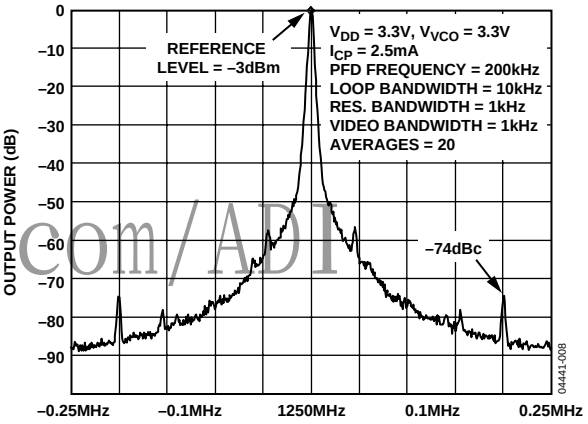

Figure 8. Reference Spurs at 500 MHz (200 kHz Channel Spacing, 10 kHz Loop Bandwidth)

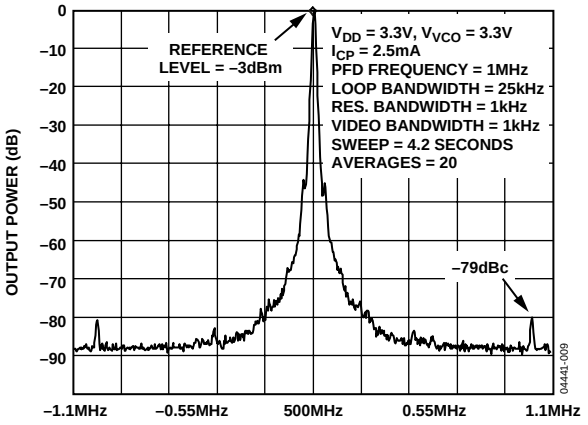

Figure 9. Reference Spurs at 500 MHz (1 MHz Channel Spacing, 25 kHz Loop Bandwidth)

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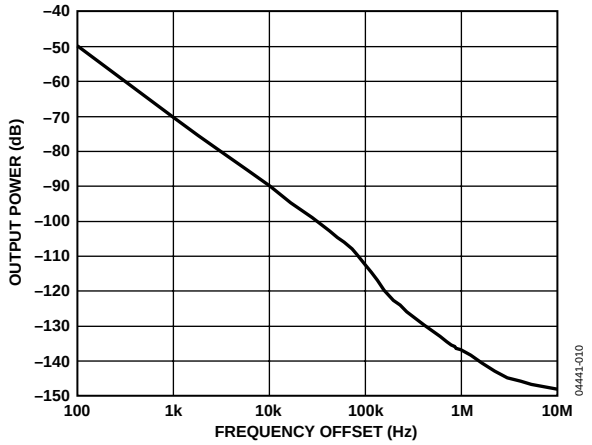

Figure 10. Open-Loop VCO Phase Noise, L1 and L2 = 1.0 nH

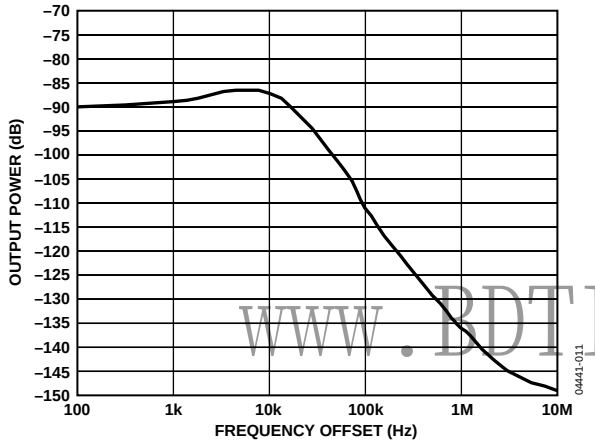

Figure 11. VCO Phase Noise, 1250 MHz, 200 kHz PFD, 10 kHz Loop Bandwidth

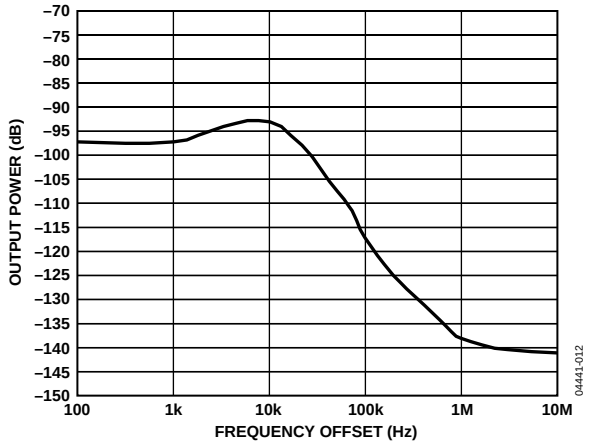

Figure 12. VCO Phase Noise, 625 MHz,
Divide-by-2 Enabled 200 kHz PFD, 10 kHz Loop Bandwidth

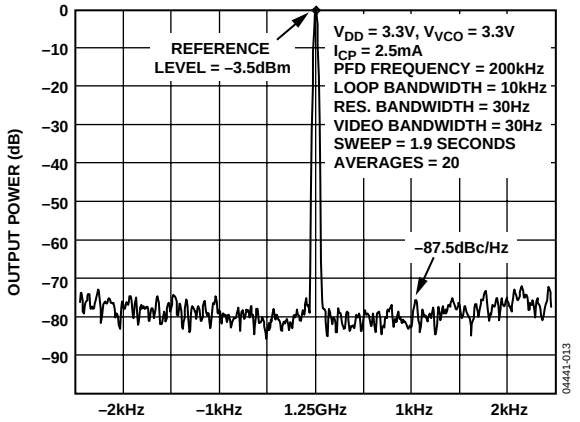

Figure 13. Close-In Phase Noise at 1250 MHz (200 kHz Channel Spacing)

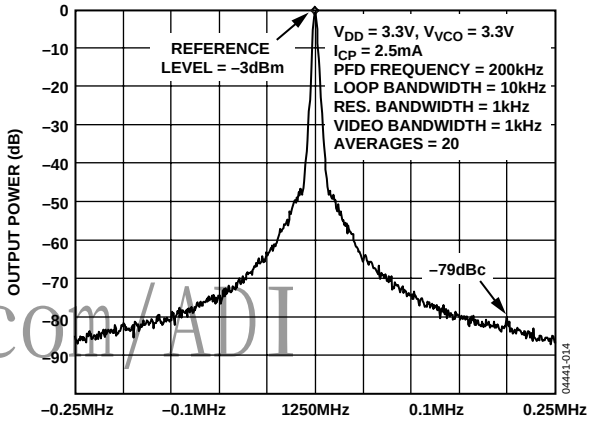

Figure 14. Reference Spurs at 1250 MHz
(200 kHz Channel Spacing, 10 kHz Loop Bandwidth)

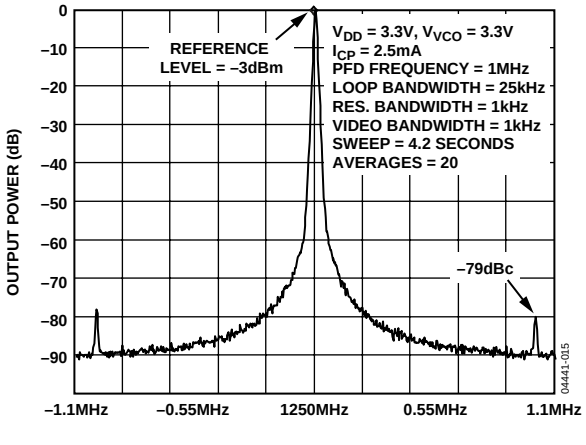

Figure 15. Reference Spurs at 1250 MHz
(1 MHz Channel Spacing, 25 kHz Loop Bandwidth)

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CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 16. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

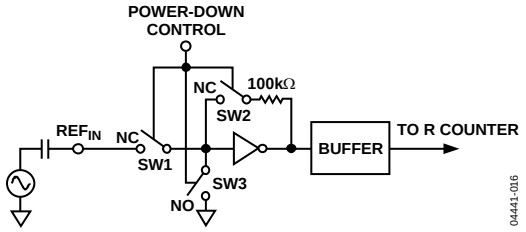

Figure 16. Reference Input Stage

PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the VCO and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9 or 16/17 and is based on a synchronous 4/5 core. A value of 32/33 can be programmed but it is not useful on this part. There is a minimum divide ratio possible for fully contiguous output frequencies; this minimum is determined by P, the prescaler value, and is given by ($P^2 - P$).

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide range division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with a VCO frequency of 2.5 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid. At fundamental VCO frequencies less than 700 MHz, a value of 8/9 is best.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The VCO frequency equation is

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

where:

f_{VCO} is the output frequency of the VCO.
P is the preset modulus of the dual-modulus prescaler (8/9 or 16/17).
B is the preset divide ratio of the binary 13-bit counter (3 to 8191).
A is the preset divide ratio of the binary 5-bit swallow counter (0 to 31).
f_{REFIN} is the external reference frequency oscillator.

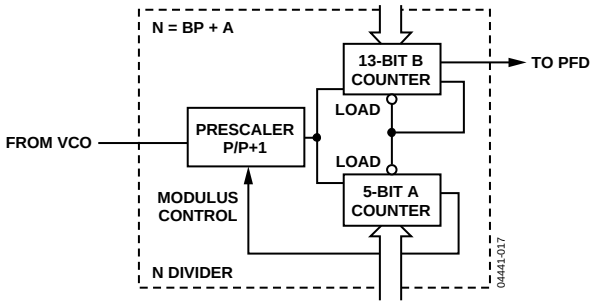

Figure 17. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PFD AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter ($N = BP + A$) and produces an output proportional to the phase and frequency difference between them. Figure 18 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the R counter latch, ABP2 and ABP1, control the width of the pulse (see Table 9).

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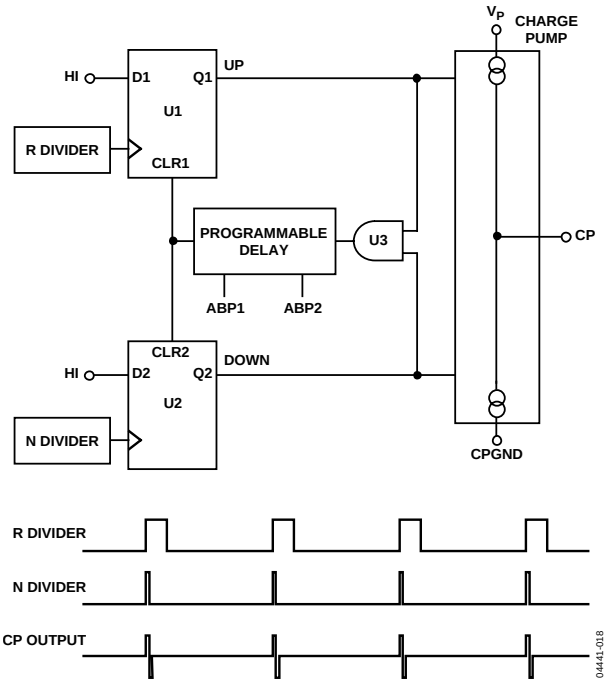

Figure 18. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4360 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. The full truth table is shown in Table 7. Figure 19 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital and analog. Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns.

With LDP set to 1, five consecutive cycles of less than 15 ns phase error are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When a lock has been detected, this output is high with narrow low-going pulses.

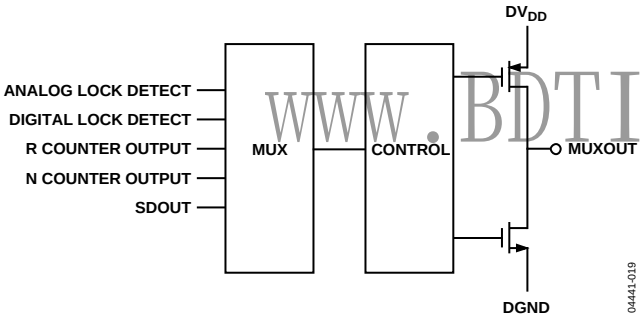

Figure 19. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4360 family's digital section includes a 24-bit input shift register, a 14-bit R counter, and an 18-bit N counter comprised of a 5-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, shown in Figure 2.

The truth table for these bits is shown in Table 5. Table 6 shows a summary of how the latches are programmed. Note that the test mode latch is used for factory testing and should not be programmed by the user.

Table 5. C2 and C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	Control Latch
0	1	R Counter
1	0	N Counter (A and B)
1	1	Test Mode Latch

VCO

The VCO core in the ADF4360 family uses eight overlapping bands, as shown in Figure 20, to allow a wide frequency range to be covered without a large VCO sensitivity (K_V) and resultant poor phase noise and spurious performance.

The correct band is chosen automatically by the band select logic at power-up or whenever the N counter latch is updated. It is important that the correct write sequence be followed at power-up. This sequence is:

1. R counter latch
2. Control latch
3. N counter latch

During band select, which takes five PFD cycles, the VCO V_{TUNE} is disconnected from the output of the loop filter and connected to an internal reference voltage.

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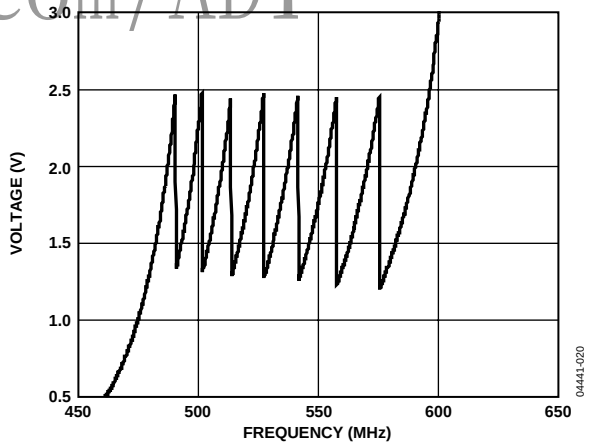

Figure 20. Frequency vs. V_{TUNE}, ADF4360-7

The R counter output is used as the clock for the band select logic and should not exceed 1 MHz. A programmable divider is provided at the R counter input to allow division by 1, 2, 4, or 8 and is controlled by Bits BSC1 and BSC2 in the R counter latch. Where the required PFD frequency exceeds 1 MHz, the divide ratio should be set to allow enough time for correct band selection.

After band selection, normal PLL action resumes. The value of K_V is determined by the value of inductors used (see the Choosing the Correct Inductance section). If divide-by-2 operation has been selected (by programming DIV2 [DB22] high in the N counter latch), the value is halved. The ADF4360 family contains linearization circuitry to minimize any variation of the product of I_{CP} and K_V.

The operating current in the VCO core is programmable in four steps: 5 mA, 10 mA, 15 mA, and 20 mA. This is controlled by Bits PC1 and PC2 in the control latch.

OUTPUT STAGE

The $RF_{OUT}A$ and $RF_{OUT}B$ pins of the ADF4360 family are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 21. To allow the user to optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable via Bits PL1 and PL2 in the control latch. Four current levels may be set: 3.5 mA, 5 mA, 7.5 mA, and 11 mA. These levels give output power levels of −14 dBm, −11 dBm, −8 dBm, and −5 dBm, respectively, using a 50 Ω resistor to V_{DD} and ac coupling into a 50 Ω load. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler (see the Output Matching section).

If the outputs are used individually, the optimum output stage consists of a shunt inductor to V_{DD}.

Another feature of the ADF4360 family is that the supply current to the RF output stage is shut down until the part achieves lock as measured by the digital lock detect circuitry. This is enabled by the mute-till-lock detect (MTLD) bit in the control latch.

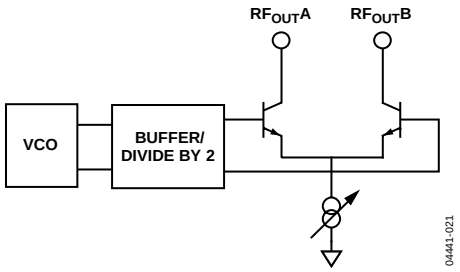

Figure 21. Output Stage ADF4360-7

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LATCH STRUCTURE

Table 6 shows the three on-chip latches for the ADF4360 family. The two LSBs decide which latch is programmed.

Table 6. Latch Structure

CONTROL LATCH

PRESCALER VALUE		POWER-DOWN 2	POWER-DOWN 1	CURRENT SETTING 2			CURRENT SETTING 1			OUTPUT POWER LEVEL		MUTE-TILL-LD	CP GAIN	CP THREE-STATE	PHASE DETECTOR POLARITY	MUXOUT CONTROL			COUNTER RESET	CORE POWER LEVEL		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

N COUNTER LATCH

DIVIDE-BY-2 SELECT	DIVIDE-BY-2	CP GAIN	13-BIT B COUNTER													RESERVED	5-BIT A COUNTER					CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DIVSEL	DIV2	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

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R COUNTER LATCH

RESERVED	RESERVED	BAND SELECT CLOCK		TEST MODE BIT	LOCK DETECT PRECISION	ANTI-BACKLASH PULSE WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV	RSV	BSC2	BSC1	TMB	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

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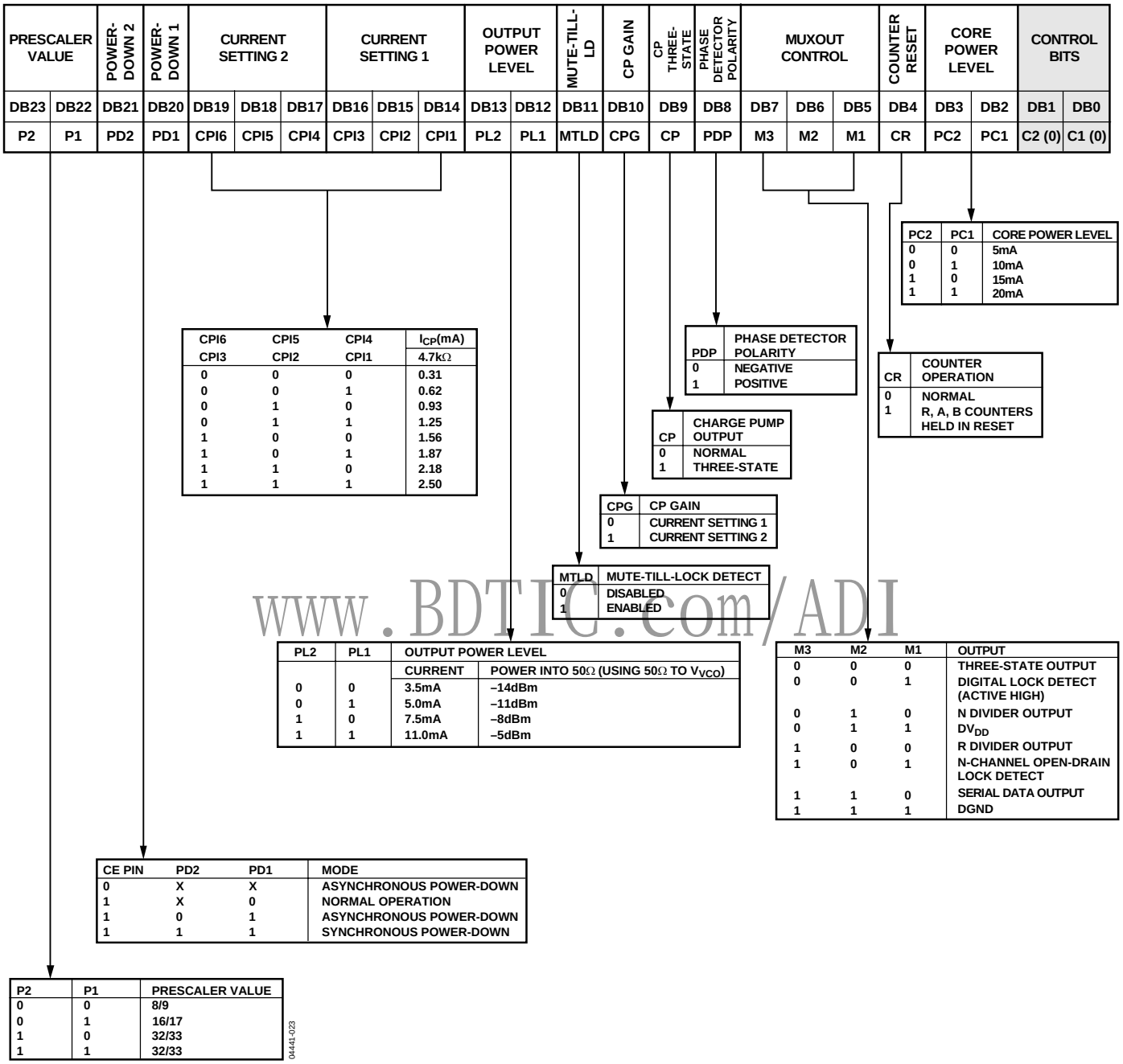
Table 7. Control Latch



PRESCALER VALUE		POWER-DOWN 2	POWER-DOWN 1	CURRENT SETTING 2			CURRENT SETTING 1			OUTPUT POWER LEVEL		MUTE-TILL-LD	CP GAIN	CP THREE-STATE	PHASE DETECTOR POLARITY	MUXOUT CONTROL			COUNTER RESET	CORE POWER LEVEL		CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

CPI6	CPI5	CPI4	I_{CP}(mA)
CPI3	CPI2	CPI1	4.7kΩ
0	0	0	0.31
0	0	1	0.62
0	1	0	0.93
0	1	1	1.25
1	0	0	1.56
1	0	1	1.87
1	1	0	2.18
1	1	1	2.50

PDP	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

CP	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

CPG	CP GAIN
0	CURRENT SETTING 1
1	CURRENT SETTING 2

MTLD	MUTE-TILL-LOCK DETECT
0	DISABLED
1	ENABLED

PL2	PL1	OUTPUT POWER LEVEL	
		CURRENT	POWER INTO 50Ω (USING 50Ω TO V_{VCO})
0	0	3.5mA	–14dBm
0	1	5.0mA	–11dBm
1	0	7.5mA	–8dBm
1	1	11.0mA	–5dBm

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

PC2	PC1	CORE POWER LEVEL
0	0	5mA
0	1	10mA
1	0	15mA
1	1	20mA

CR	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	32/33

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Table 8. N Counter Latch

DIVIDE-BY-2 SELECT	DIVIDE-BY-2	CP GAIN	13-BIT B COUNTER													RESERVED	5-BIT A COUNTER					CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DIVSEL	DIV2	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

THIS BIT IS NOT USED BY THE DEVICE AND IS A DON'T CARE BIT.

A5	A4	.....	A2	A1	A COUNTER DIVIDE RATIO
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	28
1	1	.....	0	1	29
1	1	.....	1	0	30
1	1	.....	1	1	31

B13	B12	B11	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	1	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

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F4 (FUNCTION LATCH) FASTLOCK ENABLE	CP GAIN	OPERATION
0	0	CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED
0	1	CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED

N = BP + A; P IS PRESCALER VALUE SET IN THE CONTROL LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF ($N \times F_{REF}$), AT THE OUTPUT, N_{MIN} IS (P^2–P).

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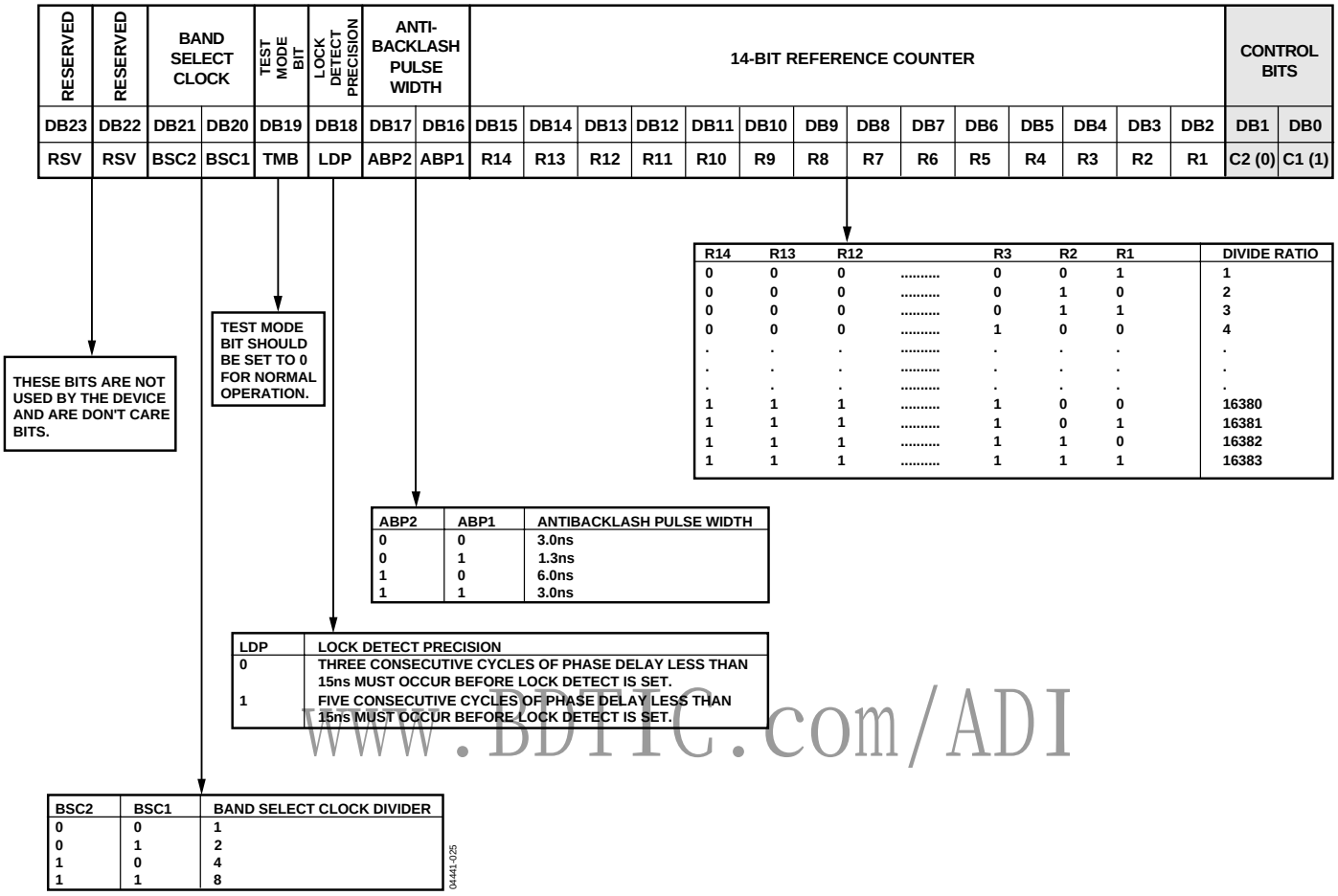
DIV2	DIVIDE-BY-2
0	FUNDAMENTAL OUTPUT
1	DIVIDE-BY-2

DIVSEL	DIVIDE-BY-2 SELECT (PRESCALER INPUT)
0	FUNDAMENTAL OUTPUT SELECTED
1	DIVIDE-BY-2 SELECTED

Table 9. R Counter Latch


RESERVED
RESERVED
BAND SELECT CLOCK
TEST MODE BIT
LOCK DETECT PRECISION
ANTI-BACKLASH PULSE WIDTH
14-BIT REFERENCE COUNTER
CONTROL BITS
DB23 DB22 DB21 DB20 DB19 DB18 DB17 DB16 DB15 DB14 DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
RSV RSV BSC2 BSC1 TMB LDP ABP2 ABP1 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4 R3 R2 R1 C2 (0) C1 (1)
THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.
TEST MODE BIT SHOULD BE SET TO 0 FOR NORMAL OPERATION.
R14 R13 R12 ..... R3 R2 R1 DIVIDE RATIO
0 0 0 ..... 0 0 1 1
0 0 0 ..... 0 1 0 2
0 0 0 ..... 0 1 1 3
0 0 0 ..... 1 0 0 4
1 1 1 ..... 1 0 0 16380
1 1 1 ..... 1 0 1 16381
1 1 1 ..... 1 1 0 16382
1 1 1 ..... 1 1 1 16383
ABP2 ABP1 ANTIBACKLASH PULSE WIDTH
0 0 3.0ns
0 1 1.3ns
1 0 6.0ns
1 1 3.0ns
LDP LOCK DETECT PRECISION
0 THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1 FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
BSC2 BSC1 BAND SELECT CLOCK DIVIDER
0 0 1
0 1 2
1 0 4
1 1 8
04441-025

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POWER-UP

Power-Up Sequence

The correct programming sequence for the ADF4360-7 after power-up is:

1. R counter latch
2. Control latch
3. N counter latch

Initial Power-Up

Initial power-up refers to programming the part after the application of voltage to the AV_{DD}, DV_{DD}, V_{VCO} and CE pins. On initial power-up, an interval is required between programming the control latch and programming the N counter latch. This interval is necessary to allow the transient behavior of the ADF4360-7 during initial power-up to settle.

During initial power-up, a write to the control latch powers up the part, and the bias currents of the VCO begin to settle. If these currents have not settled to within 10% of their steady-state value, and if the N counter latch is then programmed, the VCO may not oscillate at the desired frequency, which does not allow the band select logic to choose the correct frequency band, and the ADF4360-7 may not achieve lock. If the recommended interval is inserted, and the N counter latch is programmed, the band select logic can choose the correct frequency band, and the part locks to the correct frequency.

The duration of this interval is affected by the value of the capacitor on the C_N pin (Pin 14). This capacitor is used to reduce the close-in noise of the ADF4360-7 VCO. The recommended value of this capacitor is 10 µF. Using this value requires an interval of ≥10 ms between the latching in of the control latch bits and latching in of the N counter latch bits. If a shorter delay is required, the capacitor can be reduced. A slight phase noise penalty is incurred by this change, which is further explained in the Table 10.

Table 10. C_N Capacitance vs. Interval and Phase Noise

C_N Value	Recommended Interval Between Control Latch and N Counter Latch	Open-Loop Phase Noise @ 10 kHz Offset (L1 and L2 = 1.0 nH)	Open-Loop Phase Noise @ 10 kHz Offset (L1 and L2 = 13.0 nH)
10 µF	≥10 ms	−90 dBc	−99 dBc
440 nF	≥ 600 µs	−88 dBc	−97 dBc

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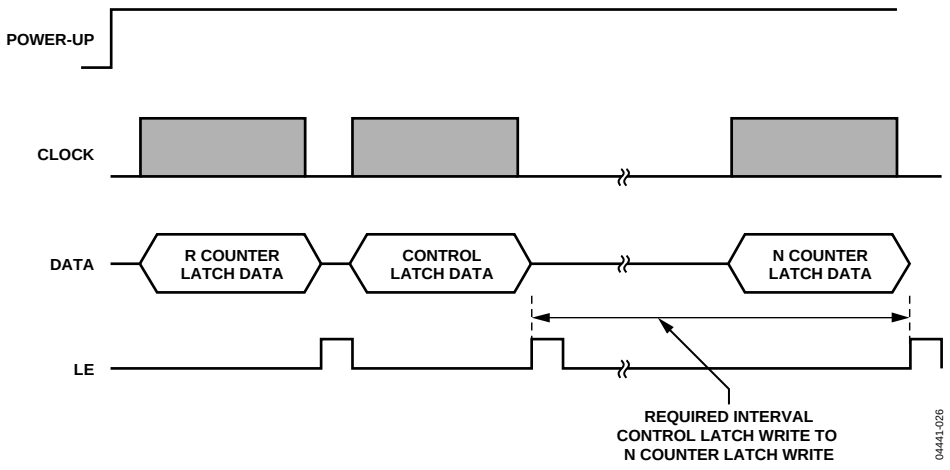

Figure 22. ADF4360-7 Power-Up Timing

Hardware Power-Up/Power-Down

If the part is powered down via the hardware (using the CE pin) and powered up again without any change to the N counter register during power-down, the part locks at the correct frequency, because the part is already in the correct frequency band. The lock time depends on the value of capacitance on the C_N pin, which is <10 ms for 10 μF capacitance. The smaller capacitance of 440 nF on this pin enables lock times of <600 μs.

The N counter value cannot be changed while the part is in power-down, since the part may not lock to the correct frequency on power-up. If it is updated, the correct programming sequence for the part after power-up is the R counter latch, followed by the control latch, and finally the N counter latch, with the required interval between the control latch and N counter latch, as described in the Initial Power-Up section.

Software Power-Up/Power-Down

If the part is powered down via the software (using the control latch) and powered up again without any change to the N counter latch during power-down, the part locks at the correct frequency, because the part is already in the correct frequency band. The lock time depends on the value of capacitance on the C_N pin, which is <10 ms for 10 μF capacitance. The smaller capacitance of 440 nF on this pin enables lock times of <600 μs.

The N counter value cannot be changed while the part is in power-down, because the part may not lock to the correct frequency on power-up. If it is updated, the correct programming sequence for the part after power-up is to the R counter latch, followed by the control latch, and finally the N counter latch, with the required interval between the control latch and N counter latch, as described in the Initial Power-Up section.

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CONTROL LATCH

With (C2, C1) = (0,0), the control latch is programmed. Table 7 shows the input data format for programming the control latch.

Prescaler Value

In the ADF4360 family, P2 and P1 in the control latch set the prescaler values.

Power-Down

DB21 (PD2) and DB20 (PD1) provide programmable power-down modes.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, with the condition that PD2 has been loaded with a 0. In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into Bit PD1 (on the condition that a 1 has also been loaded to PD2), the device goes into power-down on the second rising edge of the R counter output, after LE goes high. When the CE pin is low, the device is immediately disabled regardless of the state of PD1 or PD2.

When a power-down is activated (either synchronous or asynchronous mode), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RF outputs are debiased to a high impedance state.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

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Charge Pump Currents

CPI3, CPI2, and CPI1 in the ADF4360 family determine Current Setting 1.

CPI6, CPI5, and CPI4 determine Current Setting 2. See the truth table in Table 7.

Output Power Level

Bits PL1 and PL2 set the output power level of the VCO. See the truth table in Table 7.

Mute-Till-Lock Detect

DB11 of the control latch in the ADF4360 family is the mute-till-lock detect bit. This function, when enabled, ensures that the RF outputs are not switched on until the PLL is locked.

CP Gain

DB10 of the control latch in the ADF4360 family is the charge pump gain bit. When it is programmed to 1, Current Setting 2 is used. When it is programmed to 0, Current Setting 1 is used.

Charge Pump Three-State

This bit puts the charge pump into three-state mode when programmed to a 1. It should be set to 0 for normal operation.

Phase Detector Polarity

The PDP bit in the ADF4360 family sets the phase detector polarity. The positive setting enabled by programming a 1 is used when using the on-chip VCO with a passive loop filter or with an active noninverting filter. It can also be set to 0, which is required if an active inverting loop filter is used.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1. See the truth table in Table 7.

Counter Reset

DB4 is the counter reset bit for the ADF4360 family. When this is 1, the R counter and the A, B counters are reset. For normal operation, this bit should be 0.

Core Power Level

PC1 and PC2 set the power level in the VCO core. The recommended setting is 5 mA. See the truth table in Table 7.

N COUNTER LATCH

Table 8 shows the input data format for programming the N counter latch.

A Counter Latch

A5 to A1 program the 5-bit A counter. The divide range is 0 (00000) to 31 (11111).

Reserved Bits

DB7 is a spare bit that is reserved. It should be programmed to 0.

B Counter Latch

B13 to B1 program the B counter. The divide range is 3 (00.....0011) to 8191 (11....111).

Overall Divide Range

The overall divide range is defined by ((P × B) + A), where P is the prescaler value.

CP Gain

DB21 of the N counter latch in the ADF4360 family is the charge pump gain bit. When this is programmed to 1, Current Setting 2 is used. When programmed to 0, Current Setting 1 is used. This bit can also be programmed through DB10 of the control latch. The bit always reflects the latest value written to it, whether this is through the control latch or the N counter latch.

Divide-by-2

DB22 is the divide-by-2 bit. When set to 1, the output divide-by-2 function is chosen. When it is set to 0, normal operation occurs.

Divide-by-2 Select

DB23 is the divide-by-2 select bit. When programmed to 1, the divide-by-2 output is selected as the prescaler input. When set to 0, the fundamental is used as the prescaler input. For example, using the output divide-by-2 feature and a PFD frequency of 200 kHz, the user needs a value of N = 5,000 to generate 500 MHz. With the divide-by-2 select bit high, the user may keep N = 2,500.

R COUNTER LATCH

With (C2, C1) = (0, 1), the R counter latch is programmed. Table 9 shows the input data format for programming the R counter latch.

R Counter

R1 to R14 set the counter divide ratio. The divide range is 1 (00.....001) to 16383 (111.....111).

Antibacklash Pulse Width

DB16 and DB17 set the antibacklash pulse width.

Lock Detect Precision

DB18 is the lock detect precision bit. This bit sets the number of reference cycles with less than 15 ns phase error for entering the locked state. With LDP at 1, five cycles are taken; with LDP at 0, three cycles are taken.

Test Mode Bit

DB19 is the test mode bit (TMB) and should be set to 0. With TMB = 0, the contents of the test mode latch are ignored and normal operation occurs as determined by the contents of the control latch, R counter latch, and N counter latch. Note that test modes are for factory testing only and should not be programmed by the user.

Band Select Clock

These bits set a divider for the band select logic clock input. The output of the R counter is by default the value used to clock the band select logic, but if this value is too high (>1 MHz), a divider can be switched on to divide the R counter output to a smaller value (see Table 9).

Reserved Bits

DB23 to DB22 are spare bits that are reserved. They should be programmed to 0.

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APPLICATIONS

FREQUENCY GENERATOR

The wide frequency range of the AD4360-7, plus the on-chip divider, make it an ideal choice for implementing any general purpose clock generator or LO.

To implement a clock generator in the FM band, it is necessary to use an external divider. The ADF4007 contains a hardware-programmable N divider, allowing division ratios of 8, 16, 32, and 64. This divided-down signal is accessed from the MUXOUT pin of the ADF4007.

The minimum frequency that can be fed to the ADF4007 is 500 MHz. Therefore, 2.2 nH inductors were used to set the fundamental frequency of oscillation at 1 GHz, with a range from 950 MHz to 1100 MHz.

This allows frequencies as low as 8 MHz and as high as 137 MHz to be generated using a single system. In the circuit drawn in Figure 23, the ADF4360-7 is being used to generate 1024 MHz, and the ADF4007 is being used to divide by 8. To provide a channel spacing of 100 kHz, a PFD frequency of 800 kHz is used for the ADF4360-7 PLL. The loop bandwidth is chosen to be 20 kHz.

The output range of the system in Figure 23 is approximately 120 MHz to 135 MHz. The output phase noise is −104 dBc/Hz at 1 kHz offset. Using different inductor values allows the ADF4360-7 to be used to synthesize any different range of frequencies over the operation of the part (235 MHz to 1800 MHz).

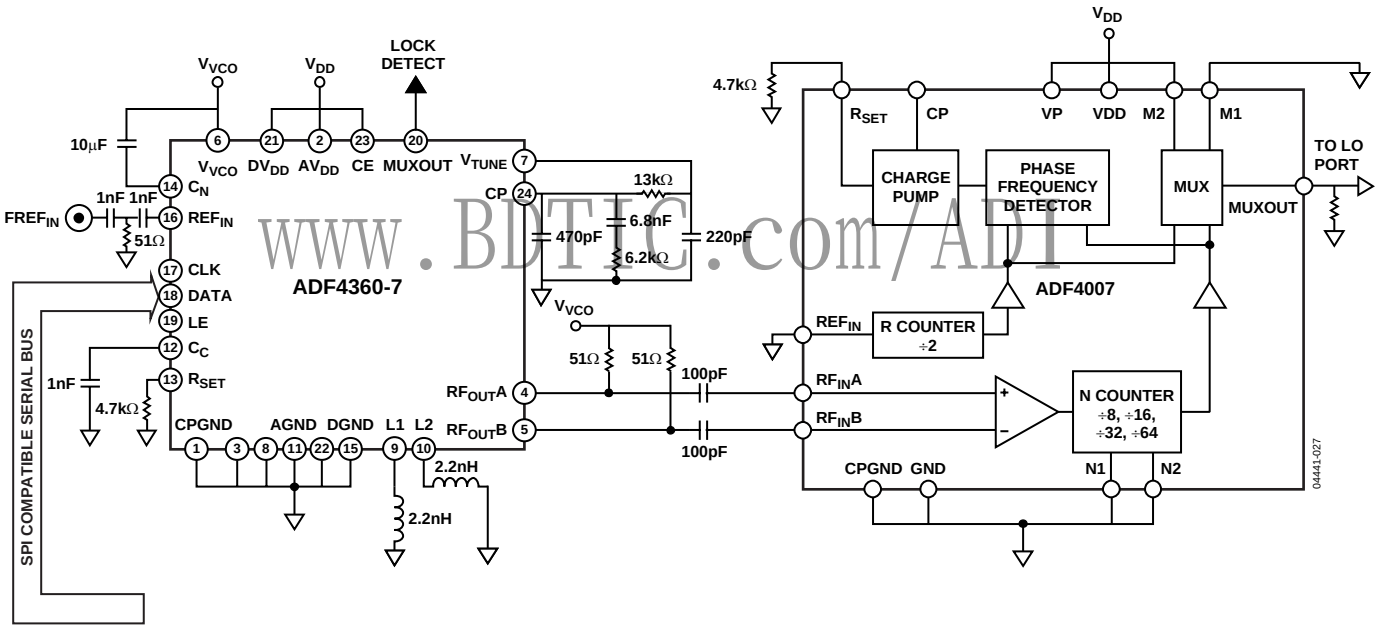

Figure 23. Frequency Generator

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CHOOSING THE CORRECT INDUCTANCE VALUE

The ADF4360-7 can be used at many different frequencies simply by choosing the external inductors to give the correct output frequency. Figure 24 shows a graph of both minimum and maximum frequency vs. the external inductor value. The correct inductor should cover the maximum and minimum frequencies desired. The inductors used are the 0402 CS type from Coilcraft. To reduce mutual coupling, the inductors should be placed at right angles to one another.

As shown in Figure 24, the lowest commercially available value of inductance, 1.0 nH, sets the center frequency at approximately 1300 MHz. For inductances less than 2.4 nH, a PCB trace should be used, a direct short. The lowest center frequency of oscillation possible is approximately 350 MHz, which is achieved using 30 nH inductors. This relationship can be expressed by

$$F_O = \frac{1}{2\pi\sqrt{6.2\text{ pF}(0.9\text{ nH} + L_{EXT})}}$$

where F_O is the center frequency, and L_{EXT} is the external inductance.

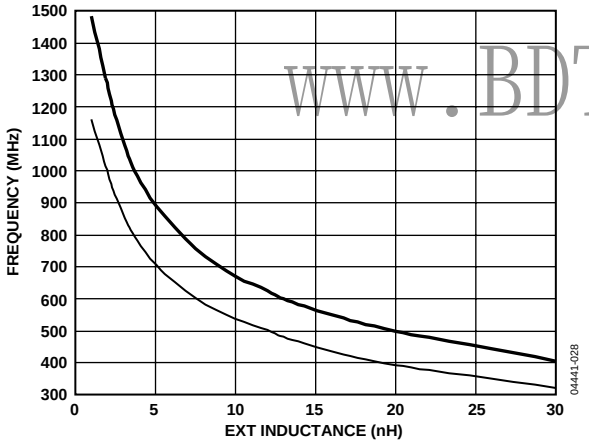

Figure 24. Output Center Frequency vs. External Inductor Value

The approximate value of capacitance at the midpoint of the center band of the VCO is 6.2 pF, and the approximate value of internal inductance due to the bond wires is 0.9 nH. The VCO sensitivity is a measure of the frequency change vs. the tuning voltage. It is a very important parameter for the low-pass filter. Figure 25 shows a graph of the tuning sensitivity (in MHz/V) vs. the inductance (nH). It can be seen that as the inductance increases, the sensitivity decreases. This relationship can be derived from the previous equation, i.e., because the inductance has increased, the change in capacitance from the varactor has less of an effect on the frequency.

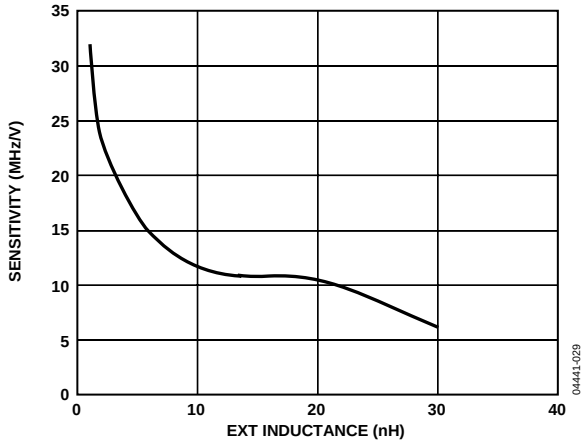

Figure 25. Tuning Sensitivity (in MHz/V) vs. Inductance (nH)

FIXED FREQUENCY LO

Figure 26 shows the ADF4360-7 used as a fixed frequency LO at 500 MHz. The low-pass filter was designed using ADIsimPLL for a channel spacing of 8 MHz and an open-loop bandwidth of 30 kHz. The maximum PFD frequency of the ADF4360-7 is 8 MHz. Because using a larger PFD frequency allows the use of a smaller N, the in-band phase noise is reduced to as low as possible, −109 dBc/Hz. The typical rms phase noise (100 Hz to 100 kHz) of the LO in this configuration is 0.3°. The reference frequency is from a 16 MHz TCXO from Fox; thus, an R value of 2 is programmed. Taking into account the high PFD frequency and its effect on the band select logic, the band select clock divider is enabled. In this case, a value of 8 is chosen. A very simple pull-up resistor and dc blocking capacitor complete the RF output stage.

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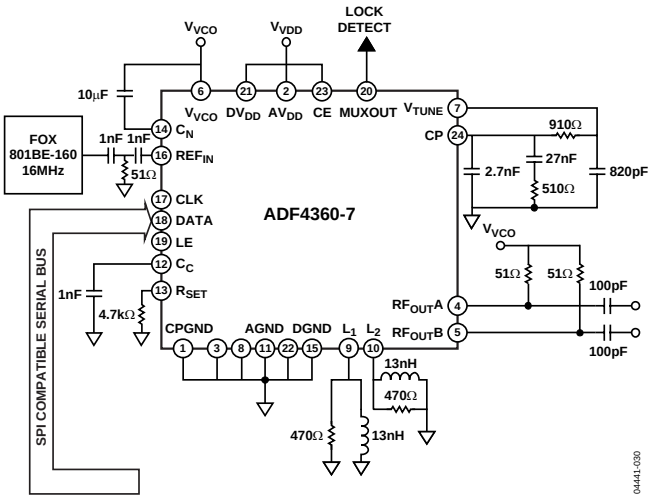

Figure 26. Fixed Frequency LO

INTERFACING

The ADF4360 family has a simple SPI®-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits that have been clocked into the appropriate register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible is 833 kHz or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 27 shows the interface between the ADF4360 family and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4360 family needs a 24-bit word, which is accomplished by writing three 8-bit bytes from the MicroConverter to the device. After the third byte has been written, the LE input should be brought high to complete the transfer.

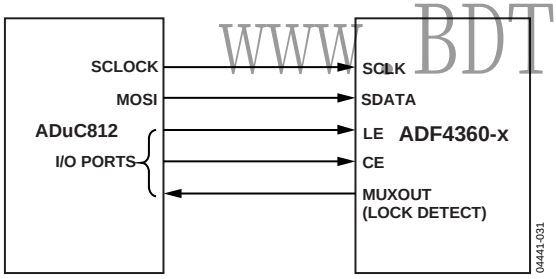

Figure 27. ADuC812 to ADF4360-x Interface

I/O port lines on the ADuC812 are also used to control power-down (CE input) and detect lock (MUXOUT configured as lock detect and polled by the port input). When operating in the described mode, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

ADSP-2181 Interface

Figure 28 shows the interface between the ADF4360 family and the ADSP-21xx digital signal processor. The ADF4360 family needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

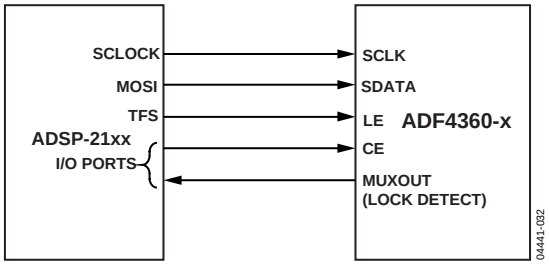

Figure 28. ADSP-21xx to ADF4360-x Interface

Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The leads on the chip scale package (CP-24) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package lead length and 0.05 mm wider than the package lead width. The lead should be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 ounce of copper to plug the via.

The user should connect the printed circuit thermal pad to AGND. This is internally connected to AGND.

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OUTPUT MATCHING

There are a number of ways to match the output of the ADF4360-7 for optimum operation; the most basic is to use a 50 Ω resistor to V_{VCO}. A dc bypass capacitor of 100 pF is connected in series, as shown in Figure 29. Because the resistor is not frequency dependent, this provides a good broadband match. The output power in this circuit typically gives −5 dBm output power into a 50 Ω load.

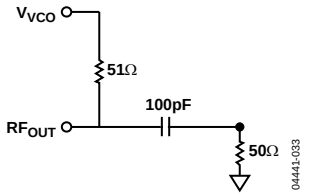

Figure 29. Simple ADF4360-7 Output Stage

A better solution is to use a shunt inductor (acting as an RF choke) to V_{VCO}. This gives a better match and, therefore, more output power. Additionally, a series inductor is added after the dc bypass capacitor to provide a resonant LC circuit. This tunes the oscillator output and provides approximately 10 dB additional rejection of the second harmonic. The shunt inductor needs to be a relatively high value (>40 nH).

Experiments have shown that the circuit shown in Figure 30 provides an excellent match to 50 Ω over a limited operating range of the ADF4360-7 (850 MHz to 950 MHz). This gives approximately −2 dBm output power across the specific frequency range of the ADF4360-7 using 3.9 nH. For other frequencies, a tuned LC is recommended. Both complementary architectures can be examined using the EVAL-ADF4360-7EB1 evaluation board.

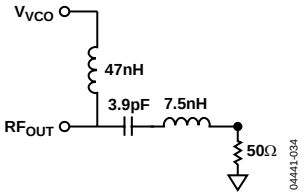

Figure 30. Optimum ADF4360-7 Output Stage

If the user does not need the differential outputs available on the ADF4360-7, the user may either terminate the unused output or combine both outputs using a balun. The circuit in Figure 31 shows how best to combine the outputs.

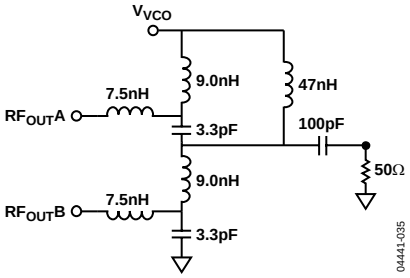

Figure 31. Balun for Combining ADF4360-7 RF Outputs

The circuit in Figure 31 is a lumped-lattice-type LC balun. It is designed for a center frequency of 900 MHz and outputs 5.0 dBm at this frequency. The series 7.5 nH inductor is used to tune out any parasitic capacitance due to the board layout from each input, and the remainder of the circuit is used to shift the output of one RF input by +90° and the second by −90°, thus combining the two. The action of the 9.0 nH inductor and the 3.3 pF capacitor accomplishes this. The 47 nH is used to provide an RF choke to feed the supply voltage, and the 100 pF capacitor provides the necessary dc block. To ensure good RF performance, the circuits in Figure 30 and Figure 31 are implemented with Coilcraft 0402/0603 inductors and AVX 0402 thin-film capacitors.

Alternatively, instead of the LC balun shown in Figure 31, both outputs may be combined using a 180° rat-race coupler.

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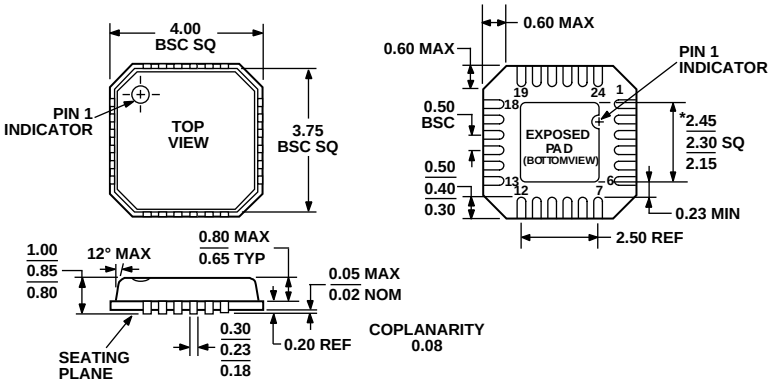
OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 32. 24-Lead Lead Frame Chip Scale Package [VQ_LFCSP]
4 mm × 4 mm Body, Very Thin Quad (CP-24-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Frequency Range	Package Description	Package Option
ADF4360-7BCP	−40°C to +85°C	350 MHz to 1800 MHz	24-Lead VQ_LFCSP	CP-24-2
ADF4360-7BCPRL	−40°C to +85°C	350 MHz to 1800 MHz	24-Lead VQ_LFCSP	CP-24-2
ADF4360-7BCPRL7	−40°C to +85°C	350 MHz to 1800 MHz	24-Lead VQ_LFCSP	CP-24-2
ADF4360-7BCPZ[1]	−40°C to +85°C	350 MHz to 1800 MHz	24-Lead VQ_LFCSP	CP-24-2
ADF4360-7BCPZRL[1]	−40°C to +85°C	350 MHz to 1800 MHz	24-Lead VQ_LFCSP	CP-24-2
ADF4360-7BCPZRL7[1]	−40°C to +85°C	350 MHz to 1800 MHz	24-Lead VQ_LFCSP	CP-24-2
EVAL-ADF4360-7EB1			Evaluation Board	

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[1]Z = Pb-free part.

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